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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,515	11/08/2001	Jay B. Reimer	TI-30113	5418

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EXAMINER	
SONG, JASMINE	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 12/04/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/008,515	REIMER ET AL.	
	Examiner	Art Unit	
	Jasmine Song	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Detailed Action

1. Claims 1-24 are represented for examination.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

3. please fill in blanks on page 2, lines 6.

4. The applicant should add the continuation statement in the first paragraph of the specification.

Drawings

5. The drawings filed on 11/08/2001 have been approved by the Examiner.

Oath/Declaration

6. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

Claim Objections

7. Claim 24 is objected to because of the following informalities

In claim 24, lines 3, "emulation logic that provides determines" should be changed to -- emulation logic that determines --.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Hedayat et al., US 6327648 B1.

Regarding claim 1, Hedayat et al teach that a digital signal processing system (col.2, lines 41-42, it is taught as a multiprocessor system) that comprises;

a shared program memory (Fig.3, it is taught as program memory of FP 202);

a plurality of processor subsystems (Fig.3, Main DSP CORE and Filter processor core) coupled to the shared program memory (Fig.3, it is taught as program memory of FP 202) to concurrently access instructions stored by the shared program memory (col.4, lines 50-52), wherein the shared program memory (program memory 202) is conditionally write-protected from at least one of the processor subsystems (it is taught

as FP program memory interface 204 allows the FP 200 to read data, col.5, lines 32-37).

Regarding claim 2, Hedayat et al teach that the program memory and the plurality of processor subsystems are fabricated on a single chip (Fig.1, it is taught as the multiprocessor computer system).

Regarding claim 3, Hedayat et al teach that the processor subsystems are prevented from writing anything to the shared program memory (it is taught as FP program memory interface 204 allows the FP 200 to read data, col.5, lines 32-37) while the processor subsystems are in a normal operating mode (it is taught as the main DSP and the FP both in the read/write operation mode).

Regarding claim 4, Hedayat et al teach that the processor subsystems are allowed to write information to the shared program memory while the processor subsystems are in an emulation mode (it is taught as the FP 200 continues execution of the instructions from its program memory 202 until it sees a STOP instruction col.6, lines 12-18).

Regarding claim 5, Hedayat et al teach that each of the plurality of processor subsystems includes:

a processor core (Fig.3, filter processor core); and

an instruction bus (the bus connected to program memory 202) that couples the processor core (filter processor core) to the shared program memory (program memory of FP 202).

Regarding claim 6, Hedayat et al teach that each of said processor cores (the main DSP core and the filter processor core) includes a bus interface module (bus interface 204) coupled to the associated instruction bus (the bus connected to program memory 202) to access instructions stored by the shared program memory (program memory 202).

Regarding claim 7, Hedayat et al teach that the bus interface module is configured to allow the processor core to perform write operations to the shared program memory only when the processor core is operating in an emulation mode (it is taught as the FP 200 continues execution of the instructions from its program memory 202 until it sees a STOP instruction col.6, lines 12-18).

Regarding claim 8, Hedayat et al. teach that the bus interface module is configured to prevent the processor core from writing anything to the shared program memory while the processor core is in a normal operating mode (it is taught as FP program memory interface 204 allows the FP 200 to read data, col.5, lines 32-37).

Regarding claim 9, Hedayat et al teach that the bus interface module is further configured to allow the processor core to write information to the shared program memory while the processor is in an emulation mode (it is taught as the FP 200 continues execution of the instructions from its program memory 202 until it sees a STOP instruction col.6, lines 12-18).

Regarding claim 10, Hedayat et al teach that the bus interface receives a signal that, when asserted, indicates that the processor core is in an emulation mode (it is taught as executing the STOP instruction will cause the FP 200 to halt the instruction execution and enter a power down mode).

Regarding claim 11, Hedayat et al teach that de-assertion of said signal causes said bus interface module to maintain an instruction bus read/write signal in a read state (it is taught as the EINT bit is set to 0), and wherein assertion of said signal causes said bus interface module to maintain the instruction bus read/write signal in accordance with shared program memory access operations requested by the processor core (it is taught as the EINT bit is set to one, the interrupt will be sent to the main DSP).

Regarding claim 12, Hedayat et al teach the processor subsystems each further include: data memory (data memory 300) coupled to the processor core via a data bus distinct from the instruction bus (Fig.3), wherein the processor core is configured to

operate on data from the data memory in accordance with program instruction retrieved via the instruction bus (col.5, lines 4-19).

Regarding claim 13, Hedayat et al teach the processor subsystems each further include: a direct memory access controller (it is well know in the memory art if the memory is the direct access memory); and a memory bus (the bus connected to the data memory 300) that couples the DMA controller to the data memory (data memory 300) and the shared program memory (program memory 202), wherein the memory bus is distinct from the instruction bus (the bus connected to the program memory) and distinct from the data bus (the data bus such as 204).

Regarding claim 14, Hedayat et al teach that the program memory is configured to service multiple instruction requests received via the instruction buses in each clock cycle (col.6, lines 46-55).

Regarding claim 15, Hedayat et al teach that the processor cores are configured to concurrently execute distinct instruction from a single program stored in the shared program memory, and wherein the order in which program instruction are executed by a processor core depends on the data that the processor core operates on (col.6, lines 61-65).

Regarding claim 16, Hedayat et al teach that a method of conditionally write protecting a shared program memory in a multi-core processor chip (col.2, lines 41-42, it is taught as a multiprocessor system), wherein the method comprises:

receiving a requested shared program memory access operation from a processor core (it is taught as the main DSP 100 downloads appropriate filter program or programs to the FP program memory, and write via the address bus to the FP program counter the start address from which to begin execution, Fig.5, step 402 to 404); and

combining the requested shared program memory access operation (the access address of FP 200) with a signal indicative of a current operating mode (the control bits) to produce a communicated shared program memory access operation (the access operation to the program memory 202), wherein when the current operating mode is a normal operating mode (it is taught as the main DSP and the FP both in the read/write operation mode), the communicated shared program memory access operation is prevented from being a write operation (it is taught as FP program memory interface 204 allows the FP 200 to read data, col.5, lines 32-37).

Regarding claim 17, Hedayat et al teach that when the current operating mode is an emulation mode (it is taught as the FP is in suspend mode, col.6, lines 15-16), the communication shared program memory access operation is always the same as the requested shared program memory access operation (it is taught as the EINT bit is set to one).

Regarding claim 18, Hedayat et al teach that the emulation mode is indicated by the assertion of a suspend signal, and wherein said combining includes:

inverting the suspend signal (it is taught as the EINT bit is set to 0); and

performing a logical OR of the inverted suspend signal with a read/write signal included in the requested access operation to produce a read/write signal for inclusion in the communicated access operation (it is taught as the main DSP 100 can write a new address into the program counter to reset interrupt and start next execution).

Regarding claim 19, Hedayat et al teach that a digital signal processor chip (col.2, lines 41-42, it is taught as a multiprocessor system) that comprises:

a volatile memory containing software instructions (Fig.3, it is taught as program memory of FP 202); and

a plurality of processor cores (Fig.3, Main DSP CORE and Filter processor core) coupled to the volatile memory (Fig.3, it is taught as program memory of FP 202) via a corresponding plurality of instruction buses (the buses connected to program memory 102 and 202), wherein the processor cores are configured to retrieve and execute instructions from the volatile memory(col.col.5, lines 46-50), and wherein during each of the instruction buses is configured to convey only read operations to the volatile memory (it is taught as FP program memory interface 204 allows the FP 200 to read data, col.5, lines 32-37) while their corresponding processor cores are in a normal

operating mode (it is taught as the main DSP and the FP both in the read/write operation mode).

Regarding claim 20, Hedayat et al teach that each of the instruction buses (the buses connected to program memory 102 and 202) includes a read/write signal line (address, data, read/write of program memory as shown in Fig.3, bus 204) that is maintained in a read state (col.5, lines 30-35) while the corresponding processor cores are in the normal operating mode (the main DSP provides data reading and writing, and FP provides data reading, col.5, lines 30-35).

Regarding claim 21, Hedayat et al teach that each of the instruction buses is configured to allow both read operations and write operations to be conveyed to the volatile memory while the corresponding processor cores are in an emulation mode (it is taught as the FP 200 continues execution of the instructions from its program memory 202 until it sees a STOP instruction col.6, lines 12-18).

Regarding claim 22, Hedayat et al teach that each of the instruction buses includes a read/write signal line having a value produced by a logic gate that combines a read/write signal value from the corresponding processor core with an operating mode signal value for the corresponding processor core (it is taught as the main DSP 100 can write a new address into the program counter to reset interrupt and start next execution).

Regarding claim 23, Hedayat et al teach that the operating mode signal acts as a gate control signal that prevents the read/write signal from the corresponding processor core from affecting the read/write signal on the instruction bus (it is taught as FP program memory interface 204 allows the FP 200 to read data, col.5, lines 32-37).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hedayat et al., US 6327648 B1 as applied to claim 22 and further in view of Chauvel et al., U.S. 6430664 B1.

Regarding claim 24, Hedayat et al teach the claimed invention as shown above, Hedayat does not teach a DSP further comprising a test port; emulation logic that determines the operating mode signals for each of the processor cores in response to control information received via the test port. However, Chauvel teaches a test port (Fig.2); emulation logic that provides determines (Fig.2, col.3, 7-11) the operating mode signals for each of the processor cores (DSP) in response to control information received via the test port.

As taught by Chauvel, the use of the test and emulation interface has the advantages of allowing test signals and JTAG signals for testing the DSP (col.2, col.3, 7-11), therefore, improving DSP data flows to/from external memory. It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Chauvel in the system of Hedayat and have the test and emulation interface for the advantages stated above.

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Elabd	US 6526462 B1
Brown	5872993

13. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

14. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 703-305-7701. The examiner can normally be reached on 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Jasmine Song

Patent Examiner

November 28, 2003

Mano Padmanabhan 11/30/03

Supervisory Patent Examiner

Technology Center 2100